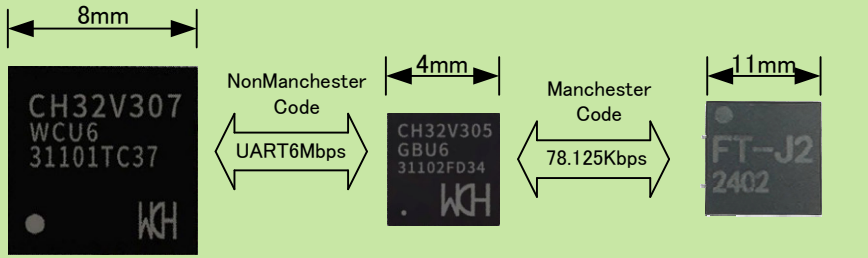
EIA709.1_Protocol_Stack_Summary

Block Diagram – Minimum Configuration



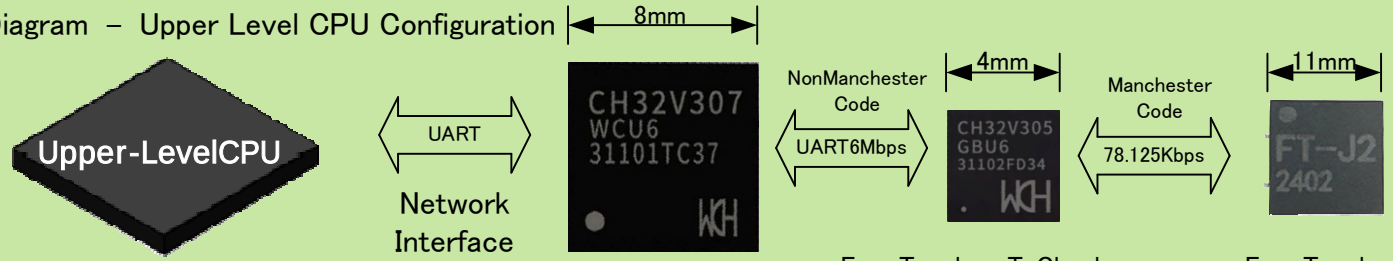
ANSI/CEA-709.1
STack Library
STACK709_CH32V
+
User APP

Free Topology TeChnology
Algorithm Stack
FT-STACK_CH32V

Free Topology
Pulse transformer
FT-J2

The EIA709.1 stack library and user application can be linked and implemented directly on a 32-bit RISC-V CPU. A low-cost yet high-performance RISC-V CPU has been selected to enable cost-effective mass production.
Application development can be carried out using the integrated development environment (IDE) “ MounRiver Studio (MRS), ” which is available for free download from the CPU manufacturer's website.
The CH32V307WCU6 is a 68-pin CPU, with more than 30 pins available for user applications.
Communication between the CPU on the STACK709_CH32V side and the Free Topology Technology Algorithm Stack (FT-STACK_CH32V) is established via a 6 Mbps UART connection.
This interface facilitates easy integration with general-purpose CPUs and uses non-Manchester encoded signals, improving overall versatility.
The FT-STACK_CH32V is implemented on the CH32V305GBU6, enabling the Free Topology Technology Algorithm Stack to be housed in a compact 4mm-square space—achieving both low cost and minimal space requirements for mass production.

Block Diagram – Upper Level CPU Configuration



Network
Interface
protocol

ANSI/CEA-709.1
Stack Library
STACK709_CH32V
+
NIP_Stack

Free Topology TeChnology
Algorithm Stack
FT-STACK_CH32V

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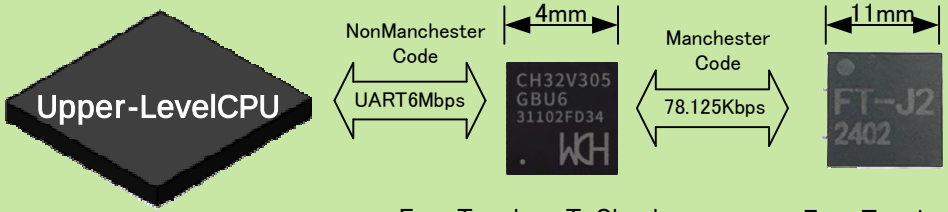
When using an upper-level CPU configuration, it is possible to develop a custom communication interface within the user application. However, by using the NIP_Stack, access to the FT-10 network becomes much easier.
We provide a Network Interface Protocol Stack (NIP_Stack) that allows for easy creation by defining information such as SNVT definitions, data types, and variable names in an INF file.

Block Diagram – General-Purpose Communication Format



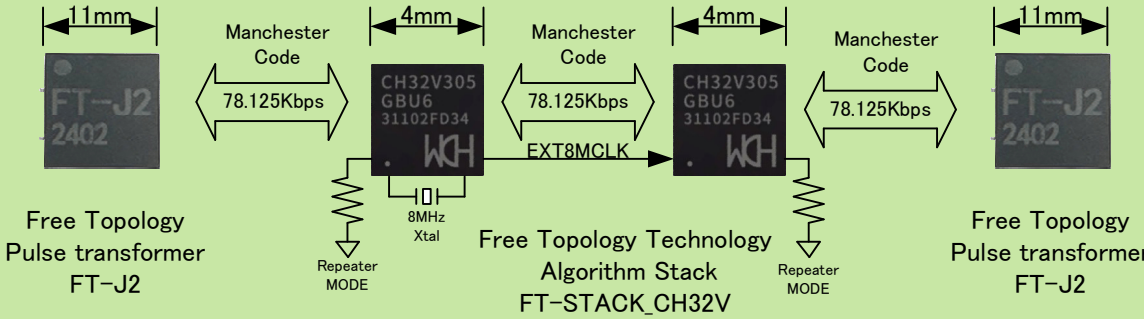
Free Topology TeChnology
Algorithm Stack
FT-STACK_CH32V

Free Topology
Pulse transformer
FT-J2

The FT-STACK_CH32V can be used not only with the EIA709.1 format but also with general-purpose communication protocols. By utilizing Free Topology Communication, long-distance transmission is now possible.
The FT-J2 pulse transformer is compliant with EIA709.3 and can be connected to an FT-10 Free Topology Network.
As a result, long-distance communication over a single-pair twisted cable using a free topology network is achievable, even in networks other than LONWORKS.

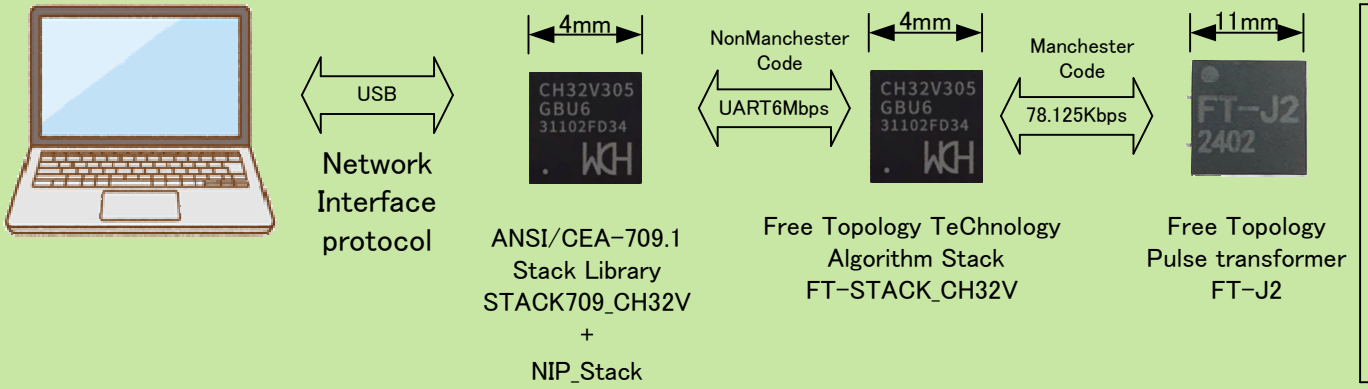
EIA709.1_Protocol_Stack_Summary

Block Diagram – FT-10 Repeater



By using two FT-STACK_CH32V modules, a repeater for the FT-10 Free Topology Network can be constructed.
The Master FT-STACK operates in XtalMode and supplies an 8MHz clock signal to the Slave FT-STACK, enabling synchronization between the CPUs . In Repeater MODE, communication is carried out using Manchester Code, which minimizes time delays and allows for extended communication distance.
If you want to minimize packet loss due to time delays, using Normal MODE instead of Repeater MODE enables FIFO communication through a message ring buffer, thereby reducing the likelihood of packet loss.

Block Diagram – USB Interface



When connecting to a host PC, a USB interface can be used for the connection. While custom development is possible, using the NIP_Stack provides easier access to the FT-10 network.
In this case, UART is not used. By porting the STACK709_CH32V along with the NIP_Stack library to the minimal configuration of the CH32V305GBU6, a 4mm-square ANSI /CEA-709.1 Stack Library can be utilized.
The host PC can access the FT-10 network by communicating through the USB interface as a virtual serial port.

License Purchase and Activation Procedure

The ANSI/CEA-709.1 Stack Library (STACK709_CH32V) and Free Topology Technology Algorithm Stack (FT-STACK_CH32V) can be downloaded free of charge from our website.
To use the library, link it with your user application and write it to either the CH32V307WCU6 or CH32V305GBU6. These libraries include protection mechanisms and require activation before use.
Licenses for activation can be purchased through our online shopping site. Once payment is confirmed, a one-time password (OTP) will be sent to the specified email address.
STACK709_CH32V activation is done using the tool EIA709ACT, and FT-STACK_CH32V activation is handled by FT709ACT. Launch the appropriate activation tool, then copy and paste the OTP into the input field.
To activate the license, you must be connected to the internet so the activation tool can communicate with our server. Once a license is obtained, local (offline) activation is also supported.
To activate a custom-developed board, a designated USB port is required. A sample circuit diagram is available on our website for reference.
Connect the target board ' s USB port to your PC ' s USB port, launch the activation tool, and complete the activation process.
Once activation is completed, one license will be marked as used.